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Cameron S. Gilligan

#33

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of	)	
Takeshi FUKUNAGA et al.	)	
Serial No. 08/781,920	)	Art Unit: 1762
Filed: December 30, 1996	)	Examiner: M. Padgett
For: METHOD OF FABRICATING A	)	
SEMICONDUCTOR DEVICE	)	
UTILIZING A CATALYST	)	
MATERIAL SOLUTION	)	Date: June 21, 1999

TRANSMITTAL OF VERIFIED ENGLISH TRANSLATION OF PRIORITY DOCUMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

As provided in the *Amendment*, filed April 21, 1999 in response to the Office Action of December 21, 1998, submitted herewith is a verified English translation of Japanese Priority Application No. 6-225851.

Acknowledgment is respectfully requested.

Respectfully submitted,

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MATERIAL SOLUTION	)	Date:

VERIFICATION OF TRANSLATION

Honorable commissioner of patents and Trademarks
Washington, D.C. 20231
Sir:

I, Tomoko Nishimi, Flat SEL-II 2-E, 1551, Hase, Atsugi-shi, Kanagawa-ken 243 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 6-225851 filed on August 26, 1994; and

that to the best of my knowledge and belief the following is a true and correct translation of the Japanese Patent Application No. 6-225851 filed on August 26, 1994.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 17th day of June, 1999

Name: Tomoko Nishimi

[Name of Document] Patent Application
[Reference Number] P002791-01
[Filing Date] August 26, 1994
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[Title of Invention] METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE
[Number of Claims] 16
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[List of Attachment]
[Attachment] Specification 1
[Attachment] Drawing 1
[Attachment] Abstract 1

[DOCUMENT NAME] Specification

[TITLE OF THE INVENTION] METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

[WHAT IS CLAIMED IS:]

[Claim 1] A method of manufacturing a semiconductor device, comprising the steps of:

selectively introducing a metal element for accelerating crystallization into an amorphous silicon film; and

irradiating the silicon film with laser light or intense light.

[Claim 2] A method of manufacturing a semiconductor device, comprising the steps of:

selectively introducing a metal element for accelerating crystallization into an amorphous silicon film;

irradiating the silicon film with laser light or intense light; and

subjecting the crystalline silicon film irradiated with laser light or intense light to a heat treatment.

[Claim 3] The method of claim 1 or 2 wherein the metal element is one kind or a plural kinds of elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag and Au.

[Claim 4] The method of claim 1 or 2 wherein the metal element is an interstitial element.

[Claim 5] The method of claim 1 or 2 wherein a concentration of the metal element in the film is 1×10^{15} atoms cm^{-3} to 5×10^{19} atoms cm^{-3}.

[Claim 6] The method of claim 1 or 2 wherein the irradiating with laser light or intense light is performed in a state that the sample is heated to 450 to 600°C.

[Claim 7] A manufacturing method of a semiconductor device, comprising the steps of:

in a state that a simple catalyst element for accelerating crystallization of an amorphous silicon film or a compound including the catalyst element is held in contact with the amorphous silicon film,

giving crystallinity to the amorphous silicon film by irradiating it with laser light or intense light; and

subjecting a silicon film in which the crystallinity is accelerated, to a heat treatment.

[Claim 8] A manufacturing method of a semiconductor device, comprising the steps of:

applying a solution in which a simple catalyst element for accelerating crystallization of an amorphous silicon film is dissolved or dispersed, to the amorphous silicon film; and

improving crystallinity of the silicon film by irradiating it with laser light or

intense light after the applying step.

[Claim 9] The method of claim 7 or 8 wherein the metal element is one kind or a plural kinds of elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag and Au.

[Claim 10] The method of claim 7 or 8 wherein the metal element is an interstitial element.

[Claim 11] A manufacturing method of a semiconductor device, comprising the steps of:

applying a polar solvent in which a compound including a catalyst element for accelerating crystallization of an amorphous silicon film is dissolved or dispersed, to the amorphous silicon film;

giving crystallinity to the silicon film by irradiating it with laser light or intense light; and

subjecting the silicon film in which crystallinity is accelerated, to a heat treatment.

[Claim 12] The method according to claim 11, wherein one or a plurality of polar solvents selected from the group consisting of water, alcohol, acid and ammonia water.

[Claim 13] The method according to claim 11, wherein the catalyst element is nickel in the form of a nickel compound.

[Claim 14] The method according to claim 13, wherein the nickel compound is at least one compound selected from the group consisting of nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetylacetonate, nickel 4-cyclohexylbutyrate, nickel oxide, and nickel hydroxide.

[Claim 15] A method of manufacturing a semiconductor device, comprising the steps of:

the first step of introducing a metal element for accelerating crystallization into an amorphous silicon film;

the second step of irradiating the amorphous silicon film with laser light or intense light;

the third step of subjecting the silicon film to a heat treatment; and

repeating the second and third steps two or more times in total.

[Claim 16] A method of manufacturing a plurality of thin film transistors on a substrate having an insulating surface, comprising the steps of:

forming an amorphous silicon film on the substrate having the insulating surface;

selectively introducing a metal element for accelerating crystallization of silicon into the amorphous silicon film; and

giving crystallinity to the amorphous silicon film by irradiating it with laser light.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FILED OF INDUSTRIAL USE]

The present invention relates to a semiconductor device using a semiconductor having crystallinity and a manufacturing method for the same.

[0002]

[PRIOR ART]

There are known thin film transistors using a thin film semiconductor (referred to hereinafter as TFTs or the like). These TFTs are constituted by using the thin film semiconductor formed over a substrate. These TFTs are used for various integrated circuits, and particularly, they attract much attention as switching elements provided for each pixel of an electro-optical device, particularly an active matrix type liquid crystal display device and as driver elements formed in its peripheral circuit portion.

[0003]

As a thin film semiconductor used for the TFTs, it is convenient to use an amorphous silicon film, however, it has a problem of poor electrical characteristics. In order to improve the characteristics of the TFT, a silicon thin film having crystallinity may be used. The silicon film having crystallinity is referred to as polycrystalline silicon, polysilicon, microcrystalline silicon, or the like. The crystalline silicon film can be obtained by forming an amorphous silicon film at first and then crystallizing it by heating.

[0004]

However, since the crystallization by heating needs to take 20 hours or more at a heating temperature not lower than 600°C, there has a problem that it is difficult to use a glass substrate as a substrate. For example, Corning 7059 glass used for active type liquid crystal display devices, has a glass strain point of 593°C. Therefore, in the case of taking larger substrate into consideration, there arises a problem about heating at 600°C or higher. That is, if a commonly used Corning 7059 glass substrate is subjected to a heat treatment at 600°C or higher and for 20 hours or longer, shrinkage and bending of the substrate will be remarkable.

[0005]

To solve the above problem, it is necessary to perform a heat treatment at a temperature as low as possible. On the other hand, it is required that the time for the heat treatment step should be as short as possible to increase the productivity.

[0006]

Further, when an amorphous silicon film is crystallized by heating, the entire silicon film is crystallized, thereby there are problems that it is impossible to effect partial crystallization nor control the crystallinity in a particular region.

[0007]

To solve this problem, Japanese Patent Laid-Open Nos. 2-140915 and 2-260524 disclose technique of effecting selective crystallization by artificially forming a portion or region where crystalline nuclei are to be generated in an amorphous silicon

film and then subjecting the film to a heat treatment. The technique is intended to form crystalline nuclei at a prescribed portion in an amorphous silicon film.

[0008]

For example, the Japanese Patent Laid-Open No. 2-140915 discloses a technique in which an aluminum layer is formed on an amorphous silicon film, crystalline nuclei are generated in the portion where the amorphous silicon and the aluminum are contacted with each other, and crystal growth is caused to proceed from the crystalline nuclei by a heat treatment. Also, the Japanese Patent Laid-Open No. 2-260524 publication discloses a technique in which tin (Sn) is added to an amorphous silicon film by ion implantation, thereby crystalline nuclei are generated in the region added with tin.

[0009]

However, since Al and Sn are substitutional metal elements, they form an alloy with silicon and do not diffuse into a silicon film. Also, crystallization proceeds such that crystalline nuclei are generated in a portion where an alloy with silicon is formed and crystal growth is started from that portion. That is, in the case of using Al or Sn, it is characterized in that crystal growth starts from a portion where Al or Sn is introduced (that is, from an alloy layer of that element and silicon.) In general, crystallization is a two-step process consisting of generation of initial nuclei and crystal growth from the nuclei. Although Al and Sn, which are substitutional metal elements with respect to silicon, are effective in generating initial nuclei, they are not effective in crystal growth that should follow.

Therefore, when Al or Sn is used, the crystallization temperature cannot be lowered nor can the crystallization time be shortened from the case of crystallizing an amorphous silicon film simply by heating it. That is, the use of Al or Si has no advantage over the conventional step of crystallizing an amorphous silicon film simply by heating it.

[0010]

[BACKGROUND OF THE INVENTION]

In accordance with the study by the inventors of the present invention, by depositing a very small amount of an interstitial element with respect to silicon, such as nickel or palladium, on the surface of an amorphous silicon film and then heating, crystallization can be performed for about 4 hours at 550°C . In this case, the process facilitates not only the initial nucleus generating step but also the subsequent crystal growth, and can therefore greatly lower the heating temperature and shorten the heating time compared with the conventional case of using only heating.

[0011]

A small amount of the above mentioned element (catalyst element for promoting crystallization) may be introduced by plasma treatment, evaporation or ion implantation. The plasma treatment is a method in which in a parallel-plate type or positive-column-type plasma CVD device, a catalyst element is added to an amorphous silicon film by using a material containing the catalyst element as an

electrode and generating a plasma in an atmosphere of nitrogen, hydrogen, or the like.

[0012]

As the above metal element for accelerating crystallization, interstitial elements of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag and Au can be used. These interstitial elements are diffused into a silicon film in a heat treatment step. Then, crystallization of silicon proceeds as the above captioned interstitial element diffuses. That is, the interstitial metal accelerates crystallization of an amorphous silicon film by its catalytic effect wherever the element reaches.

[0013]

Therefore, crystallization can be proceeded in the manner different than in the case where crystallization gradually proceeds from crystalline nuclei. For example, where the above metal elements are introduced into an amorphous silicon film at a particular point and then a heat treatment is performed, crystallization proceeds toward the direction parallel with the film surface from the portion where the metal element was introduced. The length has over several tens of micrometers or more. Also, the metal element may be introduced into an amorphous silicon film over its entire area, thereby, the entire film can be crystallized uniformly. Of course, in this case, the entire film has a polycrystalline or microcrystalline structure, however, the structure has no clear grain boundary at a particular location. Therefore, it is possible to form devices having uniform characteristics in an arbitrary portion of the film.

[0014]

Since the interstitial elements diffuse into a silicon film quickly, introduction amount (addition amount) thereof is important. If the introduction amount is small, fine crystallinity can not be obtained because the effect of accelerating crystallization is insufficient. Conversely, if the introduction amount is too large, semiconductor characteristics of silicon are inhibited.

[0015]

Thus, there is an optimum introduction amount of each of the above-mentioned metal elements for an amorphous silicon film. For example, in the case of using Ni as a metal element for accelerating crystallization, the effect of accelerating crystallization is obtained if its concentration in a crystallized silicon film is 1×10^{15} cm^{-3} or higher, and that it is clarified that the semiconductor characteristics are not inhibited if the concentration in a crystallized silicon film is 5×10^{19} cm^{-3} or lower. The concentration as mentioned here is defined as the minimum of values obtained by SIMS (secondary ion mass spectrometry). The above-mentioned metal elements other than Ni also exhibit their effect properly in respective concentration ranges similar to that of Ni.

[0016]

In order to make the concentration of an element, such as Ni, for accelerating crystallization in a crystalline silicon film after crystallization an optimum range (in

the specification, an element for accelerating crystallization is referred to as a catalyst element), it is necessary to control the introduction amount when it is introduced into an amorphous silicon film.

[0017]

Also, in the case of using nickel as a catalyst element, the following facts have been clarified with detailed investigation of the crystallization step in which an amorphous silicon film was formed, Ni is added to the amorphous silicon film by a plasma treatment, and the a crystalline silicon is formed.

(1) When nickel is introduced into an amorphous silicon film by plasma treatment, nickel has already been intruded into a considerable depth of the amorphous silicon film before a heat treatment is performed.

(2) Initial crystalline nuclei are generated at the surface into which nickel was introduced.

(3) Crystallization proceeds even with nickel is formed on an amorphous silicon film by evaporation in the same manner as in the case of using plasma treatment.

[0018]

It is concluded from the above facts that not all of nickel introduced by plasma treatment functions effectively. That is, even if a large amount of nickel is introduced, part of it does not function sufficiently. This leads to a conclusion that points (or a surface) where nickel and silicon are contacted with each other function in low-temperature crystallization. Therefore, it is necessary that nickel be dispersed in the form of as small particles as possible, preferably in the form of atoms. That is, it is concluded that nickel should be introduced so as to be dispersed in the form of atoms at as low a concentration as possible that allows low-temperature crystallization in a portion close to the surface of an amorphous silicon film.

[0019]

The vapor deposition method is a candidate of introducing a very small amount of nickel into only a portion close to the surface of an amorphous silicon film, in other words, introducing a very small amount of catalyst element so that crystallization is accelerated only in a portion close to the surface of an amorphous silicon film. However, since the vapor deposition has a problem of low controllability, it is difficult to strictly control the introduction amount of a catalyst element.

[0020]

Further, the introduction amount of a catalyst element needs to be as small as possible, which causes a problem that crystallinity becomes impurities (translator's note: it is difficult to obtain a sufficient crystallization).

[0021]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

An object of the present invention is to achieve at least one of the following when a thin-film silicon semiconductor having crystallinity is manufactured by thermal treatment at 600°C or lower using a catalyst element:

(1) Minimizing the amount of a catalyst element by introducing it with control.

(2) Improving the productivity.

(3) Obtaining higher crystallinity than that obtained by a heat treatment.

[0022]

[MEANS TO SOLVE THE PROBLEMS]

To satisfy the above purpose, the invention provides a crystalline silicon film in the following manner.

Crystallization is further promoted by irradiation of laser light or intense light in a state that a single catalyst element or a compound including the catalyst element for accelerating crystallization of an amorphous silicon film, is held in contact with the amorphous silicon film. Thus, there can be obtained a crystalline silicon film having extremely fine crystallinity.

[0023]

As a method of introducing a catalyst element for accelerating crystallization, it is useful to apply a solution containing the catalyst element to the surface of an amorphous silicon film.

[0024]

In particular, the present invention is characterized in that a catalyst element is introduced in contact with the surface of an amorphous silicon film. This is very important in controlling the amount of the catalyst element.

[0025]

A catalyst element may be introduced into either a top or a bottom surface of an amorphous silicon film. When a catalyst element is introduced into the top surface of an amorphous silicon film, a solution containing the catalyst element may be applied to the amorphous silicon film after the amorphous silicon film is formed. When the catalyst element is introduced into the bottom surface of an amorphous silicon film, a solution containing the catalyst element may be applied to a surface of the base film before the amorphus silicon film is formed, thereby the catalyst element is held in contact with the surface of the base film.

[0026]

The present invention is also characterized by forming an active region having at least one of PN, PI, NI, and other electrical junctions of a semiconductor device by using a crystallized crystalline silicon film. As the semiconductor device, a thin-film transistor (TFT), a diode, a photosensor, and the like can be enumerated. A resistor and a capacitor can also be formed by using the present invention.

[0027]

The following basic advantages can be obtained by using the construction of the present invention:

(a) It is possible to precisely control the concentration of a catalyst element in a solution, to thereby improve the crystallinity and reduce the amount of the element.

(b) If a solution is substantially contacted with the surface of an amorphous silicon film, the introduction amount of the catalyst element into the amorphous

silicon film is determined by the concentration of the catalyst element in the solution.

(c) Since a catalyst element absorbed on the surface of an amorphous silicon film mainly contributes to the crystallization, the catalyst element can be introduced at a minimum necessary value.

(d) A crystalline silicon film having superior crystallinity can be obtained without a high-temperature step.

[0028]

As a method of applying a solution containing an element for accelerating crystallization on an amorphous silicon film, an aqueous, organic solvent solution, or the like can be used as a solution. The term "containing" means both of a case where a catalyst element is included as a compound, and a case where it is simply dispersed in a solution.

[0029]

As the solvent containing a catalyst element, water, alcohol, acid, and ammonia water, which are polar solvents, can be used.

[0030]

Nickel is used as a catalyst and in the case of containing the nickel in the polar solvents, it is introduced in a form of nickel compound. As the nickel compounds, nickel bromide, nickel acetate, nickel oxalate, nickel carbonate, nickel chloride, nickel iodide, nickel nitrate, nickel sulfate, nickel formate, nickel acetylacetonate, nickel 4-cyclohexylbutyrate, nickel oxide, and nickel hydroxide can be used.

[0031]

As the solvent containing a catalyst element, benzene, toluene, xylene, carbon tetrachloride, chloroform, and ether, which are non-polar solvents, can be used.

[0032]

In this case, nickel is introduced in a form of nickel compound. As typical nickel compounds, nickel acetylacetonate and nickel 2-ethylhexanoate can be used.

[0033]

It is effective to add a surfactant to a solution containing a catalyst element. This is intended to control absorption performance by improving adhesiveness to the surface to be coated. The surfactant may be applied in advance to the surface to be coated.

[0034]

Where a nickel simple substance is used as a catalyst element, it needs to be dissolved in acid to form a solution.

[0035]

Although the above examples are directed to the case of using a solution in which nickel as a catalyst element is completely dissolved, the present invention is not limited to such a case. That is, even though nickel is not completely dissolved, an emulsion-like material may be used in which a powder of a nickel simple substance or a nickel compound is uniformly dispersed in a dispersion medium. Alternatively, a solution for forming an oxide film may be used. As the solution,

OCD (Ohka Diffusion Source) produced by Tokyo Ohka Kogyo Co., Ltd can be used. When the OCD solution is used, a silicon oxide film can be easily formed by applying it to a surface to be coated and baking it at about 200°C. The OCD solution can be used for the present invention, because impurities can be added to it freely. In this case, an oxide film is made to contain a catalyst element, and then is disposed in contact with an amorphous film. Heating is then performed at 350 to 400°C to diffuse the catalyst element into the amorphous silicon film. After the oxide film is removed, a heat treatment for crystallization may be performed at 450 to 600°C, for instance, 550°C, for about 4 hours.

[0036]

The above also applies to cases where materials other than nickel are used as a catalyst element.

[0037]

Where nickel is used as a catalyst element for accelerating crystallization and a polar solvent such as water is used as a solution solvent for including nickel, the solution is repelled by an amorphous silicon film if the solution is directly applied to the amorphous silicon film. In such a case, it becomes possible to apply a solution uniformly by first forming a thin oxide film of 100 Å or less in thickness and then applying a solution containing a catalyst element to it. It is effective to improve wettability by adding such a material as a surfactant into the solution.

[0038]

A solution can directly be applied to the surface of an amorphous silicon film by using a non-polar solvent such as a toluene solution of nickel 2-ethylhexanoate. In this case, it is effective to apply in advance such a material as an adhesive that is used in a resist application. However, care should be taken to avoid an event that excessive application of the adhesive since it obstructs addition of a catalyst element to an amorphous silicon film.

[0039]

The amount of a catalyst element to be contained in a solution depends on the kind of solution, however, it is generally desired that the nickel amount be 1 to 200 ppm, preferably 1 to 50 ppm (in terms of weight) with respect to a solution. The nickel amount should be determined in view of a nickel concentration and resistance to hydrofluoric acid in a crystallization-completed film.

[0040]

Defects in a film can be reduced by performing a heat treatment after a crystalline silicon film is obtained by the laser light irradiation. It is preferred that this heat treatment be performed at the temperature within the range of 450 to 750°C. In the case of using a glass substrate, the temperature range should be 450 to 600°C.

[0041]

It is also effective to perform a heat treatment before the laser light irradiation. In this heat treatment, a sample is heated to 450 to 750°C, preferably 450 to 600°C.

[0042]

A pulsed oscillation type excimer laser light can be used as a laser light. For example, a KrF excimer laser (wavelength: 248 nm), XeCl excimer laser (308 nm), XeF excimer laser (351 and 353 nm), ArF excimer laser (193 nm), XeF excimer laser (483 nm), and the like can be used. The excitation method may be performed using discharge excitation, X-ray excitation, optical excitation, microwave-discharge excitation, electron beam excitation, or the like.

[0043]

Instead of irradiating a laser light, other intense light, particularly infrared light, may be applied. Infrared light is effective in selectively heating a silicon thin film formed on a glass substrate, because it is hardly absorbed by glass while easily absorbed by a silicon thin film. The method of using infrared light is called rapid thermal annealing (RTA) or a rapid thermal process (RTP).

[0044]

A heat treatment that is performed after the irradiation with laser light or intense light can reduce defects in a crystalline silicon film. Fig. 8 shows results of measurements in which spin densities of crystalline silicon films manufactured under listed conditions (column of "sample manufacturing condition") were measured by the electron spin resonance (ESR) method. Although the results of Fig. 8 were obtained in a case where a heat treatment was conducted before the laser light irradiation, similar results would be obtained even without the preliminary heat treatment.

[0045]

Heating temperatures and heating periods in a nitrogen atmosphere are shown in the column of "sample manufacturing condition" of Fig. 8, and "LC" means laser light irradiation. The samples except for a sample that is given parenthesized words "without Ni" were crystallized with nickel used as a catalyst element. The g-value is an index indicating a position of a spectrum. A g-value of 2.0055 corresponds to a spectrum due to dangling bonds. Therefore, it is understood that the spin densities shown in Fig. 8 correspond to dangling bonds in films.

[0046]

It is seen from Fig. 8 that sample 4 has the lowest spin density, which means the number of dangling bonds in the film is small; that is, the numbers of defects and level in the film are smallest. For example, by comparing sample 3 and 4, it is understood that the spin density can be reduced by about one order; that is, the numbers of defects and level in a crystalline silicon film can be reduced by more than one order by subjecting it to a heat treatment after the laser light irradiation.

[0047]

A comparison between sample 2 and 3 of Fig. 8 shows that the laser light irradiation causes almost no change of the spin density; that is, the laser light irradiation has no effect on the reduction of defects in a film. However, analyses etc. of photographs taken by a transmission electron microscope have revealed that in

some cases the laser light irradiation is very effective in promoting the crystallinity. Thus, it is concluded that the laser light irradiation is very effective in promoting the crystallinity of a crystalline silicon film that has already been crystallized by heating, and that subjecting again the crystallinity-promoted film to a heat treatment is very effective in reducing defects in the film. In this manner, a silicon film that has superior crystallinity and a low defect density can be obtained.

[0048]

Further, the present invention enables selective crystal growth by selectively applying a solution containing a metal element, i.e., by selectively introducing a metal element for accelerating crystallization. In particular, in this case, crystal growth can be proceeded from a region where the solution is applied to a region where it is not applied in the direction approximately parallel with the surface of a silicon film. In this specification, the region where crystal growth has been effected approximately in parallel with the surface of a silicon film is called a "region where crystal growth has proceeded laterally".

[0049]

It has been confirmed that the concentration of a catalyst element is low in the region where crystal growth has proceeded laterally. While a crystalline silicon film is effectively used as an active layer region of a semiconductor device, it is generally preferable that the impurity concentration in the active layer region be low. Therefore, it is effective in manufacturing a device to form an active layer region by using the said region where crystal growth has proceeded laterally.

[0050]

In the present invention, most remarkable advantages can be obtained when nickel is used as a catalyst element. There may be used one or a plurality of metal elements selected from Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, and Au.

[0051]

The method of introducing a catalyst element is not limited to the case of using a solution such as an aqueous solution or alcohol, but many substances containing a catalyst element may be used widely. For example, metal compounds and oxides containing a catalyst element may be used.

[0052]

Further, to improve the crystallization ratio, the step of irradiating with laser light or intense light and the step of heating for reducing defects in a film may alternately be repeated each other more than two times.

[0053]

[Effect]

By virtue of the effect of an interstitial element for accelerating crystallization, the crystallization of an amorphous silicon film can be performed at a low temperature in a short time. To put it concretely, a crystalline silicon film can be obtained by a heat treatment of 550°C and about 4 hours, which was impossible conventionally. An interstitial element with respect to silicon accelerates

crystallization as it diffuses through a silicon film. Therefore, a crystalline silicon film can be obtained which does not have definite crystal grain boundaries, in contrast to the case of crystal growth from crystalline nuclei.

[0054]

Further, a silicon film that is small in the number of defects and has superior crystallinity can be obtained by applying laser light or intense light to a crystalline silicon film that has been crystallized by heating with assistance of the effect of a catalyst element, and then performing an additional heat treatment.

[0055]

The laser light irradiation cannot reduce defects in a film. Further, the laser light irradiation makes the surface of a silicon film an instantaneous melting state, to cause stress in the film, and the stress may cause new defects therein. The additional heat treatment can lower the number of defects by reducing the stress, thus enabling provision of a crystalline silicon film having superior electrical characteristics.

[0056]

Embodiment 1

In this embodiment, to impart crystallinity to an amorphous silicon film, an aqueous solution containing a catalyst element for accelerating crystallization is applied to the amorphous silicon film, and then laser light irradiation is performed.

[0057]

Referring to Figs. 1, steps to the introduction of a catalyst element (nickel in this embodiment) will be described. In this embodiment, a Corning 7059 glass having a size of 100 mm x 100 mm is used as a substrate.

[0058]

First, an amorphous silicon film of 100 to 1,500 Å in thickness is formed by plasma CVD or LPCVD method. In this embodiment, a 1,000-Å-thick amorphous silicon film 12 is formed by plasma CVD. (Fig. 1 (A))

[0059]

Then, a hydrofluoric acid treatment is performed to remove stain and a natural oxide film, and an oxide film 13 of 10 to 50 Å in thickness is formed. Where stain is negligible, the natural oxide film itself may be used instead of the oxide film 13.

[0060]

Since the oxide film 13 is very thin, its precise thickness is not known. However, it is estimated to be about 20 Å. In this embodiment, the oxide film 13 is formed by 5-minute irradiation with UV light in an oxygen atmosphere. Alternatively, the oxide film 13 may be formed by thermal oxidation method or a treatment with hydrogen peroxide.

[0061]

This oxide film 13 serves to allow an acetate solution containing nickel to spread over the entire surface of the amorphous silicon film in the step of applying the acetate solution containing nickel. That is, it is formed to improve the wettability. For example, where an acetate solution is directly applied to the surface

of an amorphous silicon film, the amorphous silicon film repels the acetate solution to prevent nickel from being introduced into the amorphous silicon film through its entire surface. Thus, uniform crystallization cannot be attained.

[0062]

Then, an acetate solution is produced which contains nickel at a concentration of 25 ppm. A 2-ml droplet of an acetate solution is dropped onto the surface of the oxide film 13 that is formed on the amorphous silicon film 12, and a resulting state is kept for 5 minutes. Spin drying is then performed at 2,000 rpm for 60 seconds by using a spinner. (Figs. 1(C),(D))

[0063]

From the viewpoint of practicality, the concentration of nickel in the acetate solution should be more than 1 ppm, preferably more than 10 ppm. Where a non-polar solvent such as a toluene solution of nickel 2-ethylhexanoate, the oxide film 13 is not necessary; that is, a catalyst element can directly be introduced on a surface of the amorphous silicon film.

[0064]

By performing the step of applying the nickel solution one to several times, after the spin drying, a nickel-containing layer having an average thickness of several angstroms to several hundred angstroms can be formed on the surface of the amorphous silicon film 12. In a subsequent heating step, nickel contained in this layer diffuses into the amorphous silicon film, and serves as a catalyst for accelerating crystallization. It is noted that this layer is not always a complete film.

[0065]

The state after the application of the solution is kept for 1 minute. Although the concentration of nickel finally introduced into the silicon film 12 can be controlled by this period, the largest control factor is the concentration of the solution.

[0066]

Crystallinity is imparted to the amorphous silicon film by applying KrF excimer laser light to the sample that is heated to 550°C in a nitrogen atmosphere. The reason why the sample is heated is to enhance the crystallizing effect of the laser light irradiation. In this embodiment, by using a KrF excimer laser (wavelength: 248 nm; pulse width: 30 nsec), several shots of irradiation is performed at a power density of 200 to 350 mJ/cm^2. In this step, it is effective to increase the pulse width of the excimer laser light. This is so because the period during which the surface portion of the silicon film is melted by the laser light irradiation is elongated, to thereby accelerate crystal growth in minute portions.

[0067]

The above heating treatment may be performed at more than 450°C. However, if the temperature is low, the heating time needs to be elongated, resulting in low production efficiency. On the other hand, if the temperature is set at more than 550°C, the heat resistance problem of a glass substrate used as a substrate comes to the surface.

[0068]

Although this embodiment is directed to the case of introducing a catalyst element on a surface of the amorphous silicon film, a method of introducing a catalyst element under a surface of the amorphous silicon film may be employed. In the latter case, a catalyst element may be provided on the base film using a solution containing the catalyst element before the deposition of the amorphous silicon film.

[0069]

After the completion of the laser light irradiation, a heat treatment of 550°C and 4 hours is performed in a nitrogen atmosphere. This heat treatment may be performed in a temperature range of 450 to 600°C. The heat treatment after the laser light irradiation can reduce defects in the silicon film. Thus, there can be obtained the crystalline silicon film not only superior in crystallinity but also small in the number of defects.

[0070]

Embodiment 2

A manufacturing method of this embodiment is that, in the manufacturing method of embodiment 1, a 1,200-Å silicon oxide film is selectively formed and nickel is selectively introduced by using the silicon oxide film as a mask. Crystal growth is performed parallel with the substrate.

[0071]

Figs. 2 schematically shows a manufacturing process according to this embodiment. First, a silicon oxide film 21 having a thickness of more than 1,000 Å, of 1,200 Å in this embodiment, that is to become a mask is formed over a glass substrate (Corning 7059, 10 cm x 10 cm square). Experiments by the inventors have proved that there occurs no problem even if the silicon oxide film 21 is 500 Å. It appears that the silicon oxide film can further be thinned if the film quality is fine.

[0072]

The silicon oxide film 21 is then shaped into a desired pattern by ordinary photolithography patterning process. And a thin silicon oxide film 20 is formed by 5-minute irradiation with ultraviolet light in an oxygen atmosphere. The thickness of the silicon oxide film 20 is estimated to be about 20 to 50 Å (see Fig. 2(A)). Considering the need of the silicon oxide film for improving wettability, if the size of a solution is in correspondence with the size of a pattern, there is a possibility that the solution is suitably applied to the surface of the silicon by only the hydrophilic property of the silicon oxide film as a mask. However such a case is special. In general, it is more reliable to use the silicon oxide film 20.

[0073]

In this state, as in the case of Embodiment 1, a 5-ml droplet (for the substrate of 10 cm square) of an acetate solution containing nickel at 100 ppm is dropped. To form a uniform liquid film over the entire substrate surface, spin coating is performed at 50 rpm for 10 seconds by using a spinner. After the resulting state is held for 5 minutes, spin drying is performed at 2,000 rpm for 60 seconds by using

the spinner. Alternatively, this state may be held on the spinner while being rotated at 0 to 150 rpm. (Fig. 2(B))

[0074]

Subsequently, the amorphous silicon film 12 is crystallized by performing a heat treatment of 550°C for 4 hours in a nitrogen atmosphere. In this step, crystal growth proceeds laterally, as indicated by arrows 23, from a region having a portion 22 through which nickel has been introduced to regions where nickel has not been introduced. In Fig. 2(C), reference numerals 24 and 25 denote the region that is crystallized with direct introduction of nickel and the regions in which crystallization proceeds laterally, respectively. It has been confirmed that in the regions 25 the crystallization proceeds approximately in the direction of <111> axis. It has also been confirmed by taking TEM (transmission electron microscope) photographs that in the regions 25 the crystal growth proceeds in the form of columns or branches that are parallel with the substrate.

[0075]

The crystallinity of the silicon film 12 is further improved by irradiating it with XeCl laser (wavelength: 308 nm) after the above crystallization step by the heat treatment. By the laser light irradiation in this step, crystallization between the columns or between the branches in which crystal growth has proceeded parallel to the substrate by the preceding heat treatment. That is, the crystallization ratio of the silicon film 12 can be increased. In this manner, the crystallinity of the regions 25 in which crystal growth has proceeded laterally can be improved greatly.

[0076]

It is effective to heat the substrate or the laser light surface to be irradiated in the above laser light irradiation step. It is preferred that the heating temperature be 450 to 600°C.

[0077]

After the laser light irradiation, a heat treatment is performed at 550°C for 4 hours in a nitrogen atmosphere, to further reduce defects in the film.

[0078]

In this embodiment, by changing the solution density and the holding time, the nickel concentration in the region where nickel is directly introduced can be controlled within 1×10^{16} atoms cm^{-3} to 1×10^{19} atoms cm^{-3}. Similarly, it is possible to control the nickel concentration in the lateral growth region within a range lower than the above range.

[0079]

The crystalline silicon film that has been formed by the method of this embodiment has an advantage of superior hydrofluoric acid resistance. According to the knowledge of the present inventors, crystalline silicon films that have been formed by introducing nickel by plasma processing and then performing crystallization have low hydrofluoric acid resistance.

[0080]

For example, there is a case where a silicon oxide film functioning as a gate insulating film or an interlayer insulating film is formed over a crystalline silicon film, and then electrode needs to be formed after a hole opening step for the electrode formation. In such a case, a step of removing the silicon oxide film with buffer hydrofluoric acid is usually employed. However, there is a problem that where the crystalline silicon film has low hydrofluoric acid resistance, it is difficult to remove only the silicon oxide film, and the crystalline silicon film is undesirably etched.
[0081]

However, where the crystalline silicon film has a hydrofluoric acid resistance, the difference between the etching rates of the silicon oxide film and the crystalline silicon film (selection ratio) can be made large and therefore only the silicon oxide film can be removed selectively, providing a very advantageous manufacturing step.
[0082]

As described above, since the region where crystal growth has proceeded laterally has a low catalyst element concentration and superior crystallinity, it is very effective to use this region as an active region of a semiconductor device, for instance, as a channel forming region of a thin-film transistor.
[0083]

Embodiment 3

This embodiment is directed to the case of forming a TFT by using a crystalline silicon film that is formed by the method of present invention. The TFT of this embodiment can be used in a driver circuit and a pixel area of an active matrix type liquid crystal display device. It goes without saying that the TFT can be applied to not only liquid crystal display devices but also generally called thin-film integrated circuits.
[0084]

Figs. 3 schematically show a manufacturing process according to this embodiment. First, a 2,000-Å-thick undercoat silicon oxide film (not shown) is formed on a glass substrate to prevent impurity diffusion from the glass substrate.
[0085]

A 500-Å-thick amorphous silicon film is then formed in the same manner as in Embodiment 1. After a hydrofluoric acid treatment for removing a natural oxide film, a thin oxide film of about 20 Å in thickness is formed by irradiation with ultraviolet light in an oxygen atmosphere. Alternatively, the thin oxide film may be formed by a hydrogen peroxide water treatment or thermal oxidation.
[0086]

Then, an acetate solution containing nickel at 10 ppm is applied. After holding the above state for 5 minutes, spin drying is performed by using a spinner. The silicon oxide films 20 and 21 are then removed with buffer hydrofluoric acid. Further, in a state that the sample is heated to 500°C, the crystallinity of the silicon film is enhanced by irradiation with KrF excimer laser light of 200 to 300 mJ. A crystalline silicon film can be obtained by this step.

[0087]

Subsequently, the crystallized silicon film is patterned into an island-like region 104, which is to constitute an active layer of a TFT. A silicon oxide film 105 having a thickness of 200 to 1,500 , 1,000 in this embodiment, is then formed to serve also as a gate insulating film. (Fig. 3(A))

[0088]

Attention should be paid in forming the silicon oxide film 105. In this embodiment, as material, TEOS is decomposed and formed by being subjected, together with oxygen, to RF plasma CVD method in a state that the substrate temperature is set at 150 to 600°C, preferably 300 to 450°C. The pressure ratio of TEOS to oxygen is selected to be 1:1 to 1:3. The pressure and the RF power are set at 0.05 to 0.5 torr and 100 to 250 W, respectively. Alternatively, a silicon oxide film may be formed by subjecting, as material, TEOS and an ozone gas reduced-pressure CVD method or normal-pressure CVD method in a state that the substrate temperature is set at 350 to 600°C, preferably 400 to 550°C. After the deposition of the film, it is annealed at 400 to 600°C for 30 to 60 minutes in an oxygen or ozone atmosphere.

[0089]

The crystallinity of the silicon region 104 may be enhanced in this state by irradiation with KrF excimer laser (wavelength: 248 nm; pulse width: 20 nsec) or intense light equivalent thereto. In particular, RTA (rapid thermal annealing) using infrared light is effective in manufacturing an insulated gate type electric field effect semiconductor device, not only because it can selectively heat the silicon without heating the glass substrate but also because interface levels between the silicon and the silicon oxide film can be reduced.

[0090]

After the laser light irradiation, a heat treatment is performed at 550°C for 4 hours in a nitrogen atmosphere.

[0091]

Subsequently, an aluminum film having a thickness of 2,000 Å to 1 μm is formed by electron beam evaporation, and then patterned into a gate electrode 106. Scandium (Sc) may be doped into aluminum in advance at 0.15 to 0.2 wt%. The substrate is then immersed in an ethylene glycol solution (pH approximately 7) containing 1 to 3% tartaric acid , and subjected to anodic oxidation in which platinum is used as the cathode and the aluminum gate electrode is used as the anode. The anodic oxidation is performed such that in the initial stage the voltage is raised to 220 V with a constant current and this state is kept for 1 hour until the end of the anodic oxidation. In this embodiment, with the constant current state, the appropriate voltage raising rate is 2 to 5 V/min. In this manner, an anodic oxide 109 having a thickness of 1,500 to 3,500 Å, for instance, 2,000 Å is formed. (Fig. 3(B))

[0092]

Thereafter, impurities (phosphorus) are doped into the island-like silicon film

of each TFT by ion doping (also called plasma doping) in a self-aligned manner with the gate electrode portion used as a mask. Phosphine (PH_3) is used as a doping gas, and the dose is set at 1 to 4 x 10^{15} cm^{-2}.

[0093]

Further, as shown in Fig. 3(C), the portions whose crystallinity has been degraded by the introduction of impurity region above are improved in crystallinity by irradiation with KrF excimer laser (wavelength: 248 nm; pulse width: 20 nsec). The laser energy density is set at 150 to 400 mJ/cm^2, preferably 200 to 250 mJ/cm^2. In this manner, N-type impurity (phosphorus) regions 108 and 109 are formed, which has a sheet resistance of 200 to 800 Ω/square.

[0094]

In the above step, instead of using laser light, intense light equivalent to laser light can be used. By using a flash lamp the temperature of a silicon monitor is increased to 1,000 to 1,200°C in a short period, and the sample is heated. This is RTA (rapid thermal annealing), which is also called a RTP (rapid thermal process).

[0095]

Subsequently, a 3,000-Å-thick silicon oxide film is formed, as an interlayer insulator 110 over the entire surface by plasma CVD method in which a material of TEOS is used together with oxygen, or reduced-pressure CVD method or normal-pressure CVD method in which TEOS is used as material together with ozone. The substrate temperature is set at 250 to 450°C, for instance, 350°C. After the deposition, the silicon oxide film is polished mechanically to obtain a flat surface. (Fig. 3(D))

[0096]

As shown in Fig. 1(E), contact holes for the source and drain of the TFT are formed by etching the interlayer insulator 110 and wiring lines 112 and 113 of chrome or titanium nitride are formed.

[0097]

Conventionally, it frequently occurs that a crystalline silicon film into which nickel has been introduced by a plasma treatment is etched in the above contact-hole forming step, because the crystalline silicon film has lower selectivity for buffer hydrofluoric acid than a silicon oxide film.

[0098]

However, according to this embodiment in which nickel is introduced by using the aqueous solution of a low concentration of 10 ppm, the contact holes can be formed stably with high reproducibility by virtue of high hydrofluoric acid resistance.

[0099]

Finally, the annealing is performed at 300 to 400°C for 1 to 2 hours in hydrogen, to complete hydrogenation of silicon. Thus, the TFT is completed. And an active matrix type liquid crystal display device is formed by a number of TFTs arranged in matrix which are produced at the same time. The TFT has the source and drain regions 108 and 109 and a channel forming region 114. Reference numeral

115 denotes an electrical junction portion of NI.

[0100]

Where the method of this embodiment is employed, the nickel concentration in the active layer is estimated to be about 3×10^{18} cm^{-3}, or in a lower range of 1×10^{16} atoms cm^{-3} to 3×10^{18} atoms cm^{-3}.

[0101]

Embodiment 4

This embodiment is directed to a case of forming an electronic device by using regions where crystal growth has proceeded laterally (i.e., parallel with the substrate) from a portion where nickel has been introduced selectively, as in the case of Embodiment 2. By employing such a method, the nickel concentration in the device active layer region can further be reduced, which is extremely preferable in terms of the electrical stability and the reliability of the device.

[0102]

Figs. 4 show manufacturing processes according to this embodiment. First, after a substrate 201 is cleaned, a 2,000 Å thick silicon oxide undercoat film 202 is formed by plasma CVD method with TEOS (tetraethoxysilane) and oxygen used as material gases. Then, an intrinsic (I-type) amorphous silicon film 203 having a thickness of 500 to 1,500 Å, for instance, 1,000 Å is formed by plasma CVD method. Next, a silicon oxide film 205 having a thickness of 500 to 2,000 Å, for instance, 1,000 Å are sequentially formed by plasma CVD method. The silicon oxide film 205 is selectively etched to form a region 206 where amorphous silicon is exposed.

[0103]

Thereafter, a solution (acetate solution in this embodiment) containing nickel as a catalyst element for accelerating crystallization is applied by the method of Embodiment 2. The nickel concentration in the acetate solution is 100 ppm. The other detailed procedure and conditions are the same as in Embodiment 2. Alternatively, this step may be performed according to the method of Embodiment 3 or Embodiment 4.

[0104]

Subsequently, the silicon film 203 is crystallized by scanning it with laser light that has been formed in a line to a leftward direction on the drawing sheet starting from a region 206. The linear laser light extends to the depth direction of the figure. The width of the laser light is several millimeters to several centimeters in the longitudinal direction, and the length is tens of centimeters. This laser light irradiation step is performed in a state that the sample is heated to 550°C.

[0105]

By performing the above laser light irradiation, crystal growth proceeds parallel with the substrate as indicated by an arrow starting from the region 206 that is in direct contact with nickel. In the region 204, nickel is directly introduced and crystallization is effected. In the region 203, crystallization proceeds laterally. The

laterally grown crystal region 203 is about several tens of micrometers long. (Fig. 4(A))

[0106]

After the above crystallization step by the heat treatment, the crystallinity of the silicon film 203 is enhanced by irradiation with infrared light having a wavelength 1.2 μm. This step is equivalent in effect to a high-temperature heat treatment for several minutes.

[0107]

A halogen lamp is used as an infrared light source. The intensity of the infrared light is adjusted so that the temperature of a monitor single crystal silicon wafer becomes 900 to 1,200°C. Concretely, the temperature of a thermocouple embedded in a silicon wafer is monitored and fed back to the infrared light source. In this embodiment, the temperature is increased at a constant rate of 50 to 200°C/sec and decreased with natural cooling at a rate of 20 to 100°C. Since the infrared light irradiation selectively heats the silicon film, the heating of the glass substrate can be minimized.

[0108]

Further, a heat treatment is performed at 550°C for 4 hours in a nitrogen atmosphere to reduce defects in the film. The silicon oxide film 205 is then removed together with the oxide film formed on the surface of the region 206. After the silicon film 204 is patterned, it is dry-etched, and an island-like active layer 208 is formed. In the region 206 shown in Fig. 4(A), nickel has been introduced directly and therefore exists at a high concentration. It is also confirmed that nickel exists at a high concentration in the end of crystal growth. The nickel concentration in these regions is higher than in the intermediate region. Therefore, in this embodiment, in the active layer 208 the high nickel concentration regions do not overlap with the channel forming region.

[0109]

Thereafter, the silicon oxide film 209 is formed by oxidizing the surface of the active layer (a silicon film) 208 left for one hour in an atmosphere of 10 atm and 500 to 600°C, typically 550°C, including water vapor of 100 volume %, so that the surface of the active layer (silicon film) 208 is oxidized to form a 1,000 Å thick silicon oxide film 209. After the silicon oxide film 209 is formed by thermal oxidation, the substrate is held at 400°C in an ammonia atmosphere (1 atm, 100%). The silicon oxide film 209 is subjected to nitriding processing by irradiating the substrate in this state for 30 to 180 seconds with infrared light having a peak in a wavelength range of 0.6 to 4 μm, for instance, 0.8 to 1.4 μm. In this step, HCl of 0.1 to 10% may be mixed into the atmosphere. (Fig. 4(B))

[0110]

Subsequently, an aluminum (containing scandium at 0.01 to 0.2%) having a thickness of 3,000 to 8,000 Å, for instance, 6,000 Å is formed by sputtering method. The aluminum film is patterned into a gate electrode 210. (Fig. 2(C))

[0111]

Further, the surface of the aluminum electrode is subjected to anodic oxidation to form a 2,000 Å thick oxide layer 211. The anodic oxidation is performed using an ethylene glycol solution containing tartaric acid at 1 to 5%. As oxide 211 becomes in thickness forming the offset gate regions in a later ion doping step, the length of offset gate regions can be determined in the above anodic oxidation step. (Fig. 4(D))

[0112]

Next, impurities (phosphorus in this embodiment) for giving N-conductive type are added by ion doping (also called plasma doping) method in a self-aligned manner to the active layer region (constituting the source, drain and channel) with the gate electrode portion (i.e., the gate electrode 210 and the oxide layer 211 surrounding it) used as a mask. Phosphine (PH_3) is used as a doping gas, and the acceleration voltage is set at 60 to 90 kV, for instance, 80 kV. The dose is set at 1×10^{15} to $8 \times 10^{15} cm^{-2}$, for instance, $4 \times 10^{15} cm^{-2}$. Thus, N-type impurity regions 212 and 213 can be formed. As is apparent from the figure, the gate electrode and the impurity regions are offset from each other by a distance x. This type of offset state is effective particularly in reducing a leak current (also called an off-current) when the reversely biased voltage (supplied with a negative voltage in the case of an N-channel TFT) is applied to the gate electrode. The offset is more effective when provided in the TFT for controlling a pixel of an active matrix as in the case of this embodiment, because in such a case the leak current is desired to be low to prevent charge stored in a pixel electrode escaping, to thereby produce superior images.

[0113]

Subsequently, annealing is effected by laser light irradiation. Although a KrF excimer laser (wavelength: 248 nm; pulse width: 20 nsec) is used in this embodiment, other lasers may also be used. As for the laser light irradiation conditions, the energy density is 200 to 400 mJ/cm^2, for instance, 250 mJ/cm^2, and 2 to 10 shots, for instance, 2 shots, are applied per one location. The effect may be enhanced by heating the substrate to about 200 to 450°C during the irradiation of the laser light. (Fig. 4(E))

[0114]

Thereafter, a 6,000 Å thick silicon oxide film 214 is formed by plasma CVD method as an interlayer insulator. Further, a transparent polyimide film 215 is formed by spin coating method to level the surface.

[0115]

After contact holes are formed in the interlayer insulator 214 and 215, electrodes and wiring lines 217 and 218 of the TFT are formed by using a metallic material such as a multilayered film of titanium nitride and aluminum. Finally, annealing is performed at 350°C for 30 minutes in a hydrogen atmosphere of 1 atm, to thereby complete a pixel circuit having TFTs of an active matrix. (Fig. 4(F))

[0116]

Since the TFT manufactured according to this embodiment can have a high mobility, it can also be used in a driver circuit of an active matrix type liquid crystal display device.

[0117]

Embodiment 5

Figs. 5 are cross-sectional drawings showing a manufacturing process according to this embodiment. First, a 2,000 Å thick silicon oxide undercoat film 502 is formed on a substrate (Corning 7059) 501 by sputtering. If the substrate is subjected, before or after the deposition of the undercoat film, to annealing at a temperature higher than the strain point and then to slow cooling to a temperature lower than the strain point at a rate of 0.1 to 1.0°C/min, its contraction in subsequent steps that are associated with a temperature increase (including a thermal oxidation step and an ensuing thermal annealing step of the invention) is reduced to facilitate mask alignment. In the case of the Corning 7059 substrate, the following procedure is recommended. The substrate is annealed at 620 to 660°C for 1 to 4 hours, then gradually cooled at a rate of 0.03 to 1.0°C/min, preferably 0.1 to 0.3°C/min, and taken out when the temperature is reduced to 400 to 500°C.

[0118]

Thereafter, an intrinsic (I-type) amorphous silicon film having a thickness of 500 to 1,500 Å, for instance, 1,000 Å, is formed by plasma CVD method. Then, nickel as a catalyst element for accelerating crystallization is introduced into the surface of the amorphous silicon film by the method described in Embodiment 1. In a state that the sample is heated to 500°C in a nitrogen atmosphere (atmospheric pressure), the amorphous silicon film is crystallized by irradiation with KrF excimer laser light. Further, a heat treatment of 550°C for 4 hours is performed in a nitrogen atmosphere. The silicon film is then patterned into the size of 10 1,000 μm square to form an island-like silicon film (an active layer of the TFT) 503. (Fig. 5(A))

[0119]

Subsequently, an oxygen atmosphere of 1 atm and 500 to 750°C (typically 600°C) which contains water vapor of 70 to 90% is formed by a pyrogenic reaction method with a hydrogen-to-oxygen ratio of 1.5 to 1.9. A silicon oxide film 504 having a thickness of 500 to 1,500 Å, for instance, 1,000 Å, is formed by oxidizing the surface of the silicon film left in such an atmosphere for 3 to 5 hours. It should be noted that the above oxidation reduces the thickness of the surface of the initial silicon film by more than 50 Å, as a result, contamination in the outermost portion of the silicon film is prevented from reaching the silicon-silicon oxide boundary. That is, the silicon-silicon oxide boundary can be made clean. A silicon oxide film is two times thicker than a silicon film to be oxidized. Therefore, where a 1,000-Å-thick silicon oxide film is produced by oxidizing a 1,000-Å-thick silicon film, the remaining portion of the silicon film will have a thickness 500 Å.

[0120]

In general, superior characteristics such as mobility improvement and off-

current reduction can be obtained as the thicknesses of the silicon oxide film (gate insulating film) and the active layer are made thinner. On the other hand, the initial amorphous silicon film can be crystallized more easily as its thickness is made larger. Thus, conventionally, there exists a contradiction between the characteristics and the process with respect to the active layer thickness. The present invention has first solved such a contradiction. That is, according to the present invention, a thick amorphous silicon film is formed before the crystallization, to obtain a superior crystalline silicon film. The silicon film is thereafter thinned by oxidation to improve the characteristics as a TFT. This thermal oxidation has an additional advantage of a reduced number of recombination centers in the active layer, because amorphous portions and crystal grain boundaries where recombination centers likely occur are oxidized more easily. This contributes to increase of a production yield.

[0121]

After the silicon oxide film 504 is formed by thermal oxidation (1 atm, 100%), the substrate is annealed at 600°C for 2 hours in a dinitrogen monoxide atmosphere. (Fig. 5(B))

Subsequently, a polycrystal silicon film (containing phosphorus at 0.01 to 0.2%) having a thickness of 3,000 to 8,000 Å, for instance, 6,000 Å, is formed by reduced-pressure CVD method. Then, by patterning the silicon film, a gate electrode 505 are formed. By using this silicon film as a mask, impurities (phosphorus in this embodiment) for giving N-conductive type to the active layer region (to constitute the source, drain and channel) are added by ion doping (also called plasma doping) method in a self-aligned manner. Phosphine (PH_3) is used as a doping gas, and the acceleration voltage is set at 60 to 90 kV, for instance, 80 kV. The dose is set at 1 x 10^{15} to 8 x 10^{15} cm^{-2}, for instance, 5 x 10^{15} cm^{-2}. Thus, N-type impurity regions 506 and 507 can be formed.

[0122]

Thereafter, annealing is performed by laser light irradiation. Although a KrF excimer laser (wavelength: 248 nm; pulse width: 20 nsec) is used in this embodiment, other lasers may also be used. As for the laser light irradiation conditions, the energy density is 200 to 400 mJ/cm^2, for instance, 250 mJ/cm^2, and 2 to 10 shots, for instance, 2 shots, are irradiated per one location. The effect may be enhanced by heating the substrate to 200 to 450°C during this laser light irradiation. (Fig. 6(C))

[0123]

This step may be performed by lamp annealing method with near infrared light. Near infrared ray is absorbed into crystallized silicon more easily than amorphous silicon, and can provide effective annealing equivalent to thermal annealing at more than 1,000°C. On the other hand, near infrared ray is hardly absorbed into a glass substrate. More specifically, although far infrared light is absorbed into a glass substrate, visible light and near infrared light (wavelength range: 0.5 to 4 μm) are hardly absorbed into it. Therefore, it isn't necessary to heat a glass substrate to a

high temperature, and allows the treatment to be completed in a short period. Thus, it can be said that this method is most suitable for steps where contraction of a glass substrate is problematic.

[0124]

Thereafter, a 6,000 Å thick silicon oxide film 508 is formed by plasma CVD method as an interlayer insulator. Also, the interlayer insulator may be made of polyimide. After contact holes are formed, electrodes and wiring lines 509 and 510 of the TFT are formed by using a metallic material such as a multilayered film of titanium nitride and aluminum. Finally, annealing is performed at 350°C for 30 minutes in a hydrogen atmosphere of 1 atm, to complete the TFT. (Fig. 6(D))

[0125]

TFTs produced by the above method had a mobility of 110 to 150 cm^2/Vs and an S-value of 0.2 to 0.5 V/figure. P-channel type TFTs produced by doping boron into the source and drain in the same manner showed a mobility of 90 to 120 cm^2/Vs and an S-value of 0.4 to 0.6 V/figure. Thus, the mobility was increased by more than 20% and the S-value was reduced by more than 20% from the case of forming the gate insulating film by known PVD method or CVD method.

Also in terms of reliability, TFTs produced according to this embodiment showed superior results not inferior to those produced by performing thermal oxidation at a temperature as high as 1,000°C.

[0126]

Embodiment 6

Figs. 6 are cross sectional drawings showing a manufacturing process according to this embodiment, which is directed to TFTs that are arranged in a pixel area of an active matrix type liquid crystal display device.

[0127]

First, a 2,000 Å thick silicon oxide undercoat film 52 is formed on a substrate (Corning 7059) 51. Further, an intrinsic (I-type) amorphous silicon film having a thickness of 200 to 1,500 Å, 800 Å in this embodiment, is formed thereon by plasma CVD method. Nickel as a catalyst element is introduced by the method of Embodiment 1, and the crystallinity of a resulting crystalline silicon film is enhanced by irradiating it with KrF excimer laser light in a state that it is heated to 550°C. Further, a heat treatment of 550°C and 4 hours in a nitrogen atmosphere is performed.

[0128]

In the crystalline silicon film thus produced, there is no clear crystal grain boundary at any particular location. Therefore, the active layer of a TFT can be formed at any location on its surface. That is, since the entire film is uniformly crystallized, properties of a crystalline silicon film that constitutes active layers of all the TFTs can be made uniform even where thin film transistor are formed in matrix. Thus, there can be obtained a number of TFTs having a small unevenness in characteristics.

[0129]

The crystalline silicon film is patterned into an island-like region 53, and a 1,000 Å thick silicon oxide film 54 is formed covering the island-like silicon region. Although the following description will be directed to the case of forming one TFT with reference to Figs. 6, actually a necessary number of TFT are formed in matrix at the same time.

[0130]

Subsequently, an aluminum film (containing scandium at 0.1 to 0.3 wt%) having a thickness of 3,000 to 8,000 Å, for instance, 6,000 Å, is formed by sputtering, and a thin anodic oxide of 100 to 400 Å in thickness is formed on the surface of an aluminum film. A photoresist of about 1 μm in thickness is formed on the thus-processed aluminum film by spin coating method. And a gate electrode 55 is formed by a known photolithography method. A photoresist mask 56 is left on the gate electrode. (Fig. 6(A))

[0131]

Thereafter, the substrate is immersed in an aqueous solution of 10% oxalic acid and anodic oxidation is effected at a constant voltage of 5 to 50 V, for instance, 8 V, for 10 to 500 minutes, for instance 200 minutes, so that a porous anodic oxide 57 of about 5,000 Å in thickness are formed on side faces of the gate electrode. Since the top surface of the gate electrode is covered with the mask material 56, almost no anodic
oxidation proceeds there. (Fig. 6(B))

[0132]

After the mask material is removed to expose the top surface of the gate electrode, the substrate is immersed in an ethylene glycol solution (pH-adjusted neutrally by use of ammonia) of 3% tartaric acid and anodic oxidation is effected such that the voltage is increased to 100 V at a rate of 1 to 5 V/min, for instance, 4 V/min, with current conduction. In this case, not only the top surface of the gate electrode but also its side faces are subjected to anodic oxidation, so that a dense, non-porous anodic oxide 58 of 1,000 Å in thickness is formed. The anodic oxide has a withstand voltage of more than 50 V. (Fig. 6(C))

[0133]

Then, the silicon oxide film 54 is etched by dry etching method. In this etching step, only the silicon oxide film is etched, and the anodic oxide 37 and 38 are not etched. The silicon oxide film under the anodic oxide is not etched and left as a gate insulating film 59. (Fig. 6(D))

[0134]

Subsequently, the porous anodic oxide 57 is etched with a mixed acid comprising phosphoric acid, phosphoric acid, acetic acid and nitric acid, to expose the non-porous anodic oxide 58. And impurities (phosphorus) are introduced into the silicon region 33 by plasma doping method with the gate electrode 35 and the side porous anodic oxide 37 used as a mask. Phosphine (PH_3) is used as a doping gas,

and the acceleration voltage is set at 5 to 30 kV, for instance, 10 kV. The dose is set at 1 x 10^{14} to 8 x 10^{15} cm^{-2}, for instance, 2 x 10^{15} cm^{-2}.

[0135]

In this doping step, phosphorus is introduced at a high concentration in regions 60 that are not covered with the gate insulating film 59. On the other hand, in a region 61 that is covered with the gate insulating film 59, the doping amount is small because the gate insulating film functions as an obstruction. In this embodiment, impurities of only 0.1 to 5% of those introduced into the region 60 are introduced. Thus, the N-type high-concentration impurity regions 60 and the low- concentration impurity region 61 are formed. (Fig. 6(E))

[0136]

Thereafter, doped impurities are activated by laser annealing in which laser light is irradiated from the top. A 6,000-Å-thick silicon oxide film 62 is then formed by plasma CVD method as an interlayer insulator. An ITO electrode 64 to become a pixel electrode is then formed. After contact holes are formed, electrodes and wiring lines 63 for the source and drain regions of the TFT are formed by using a metallic material such as a multilayered film of titanium nitride and aluminum. Finally, annealing is performed at 350°C for 30 minutes in a hydrogen atmosphere of 1 atm. In this manner, the TFT is completed. (Fig. 6(F))

[0137]

This embodiment can produce the same structure as the low concentration drain (LDD) structure. It is known that the LDD structure is effective in suppressing degradations due to hot carriers. The TFT produced according to this embodiment has the same advantage. However, the present embodiment can produce the LDD with a single doping step, which is not the case in the known process of producing the LDD. In addition, this embodiment has a feature that the high-impurity-concentration regions 60 are defined by utilizing the gate insulating film 59 that has been defined by the porous anodic oxide 57. That is, ultimately, the impurity regions are indirectly defined by the porous anodic oxide 57. As is apparent from this embodiment, the width x of the LDD region is substantially determined by the width of the porous anodic oxide.

[0138]

A higher degree of integration can be realized by using the manufacturing method of this embodiment. In such a case, it is more favorable that the width x of the offset region or the LDD region be changed in accordance with the characteristics required for the TFT. In particular, as reduction of off-current is realized, the method of this embodiment is most suitable for a TFT that is intended to hold charge in a pixel electrode.

[0139]

Embodiment 7

Fig. 7 is a block figure of an electro-optical system using an integrated circuit in which a display, CPU, memory, etc. are provided on a single glass substrate. An

input port reads an externally input signal and converts it to an image signal. A correction memory corrects an input signal etc. in accordance with the characteristics of an active matrix panel, and is therefore dedicated to the panel. In particular, this correction memory is a fixed memory that has information specific to the respective pixels to allow individual corrections for those pixels. More specifically, where an electro-optical device has a point-defect pixel, signals corrected for that pixel are supplied to pixels around that pixel, to thereby cover the point defect, i.e., make it unrecognizable. Where a certain pixel is darker than pixels around it, a larger signal is supplied to that pixel to make the brightness of it be the same level as that of the adjacent pixels.

[0140]

The CPU and the memory are of the same kinds as in an ordinary computer. In particular, the memory includes, as a RAM, an image memory corresponding to the respective pixels. Also, the intensity of back light which irradiates from the back side of the substrate can be changed in accordance with image information.

[0141]

To obtain offset regions or LDD regions suitable for the respective circuits, 3 to 10 series of wiring lines may be formed to enable the anodic oxidation conditions to be changed respectively. Typically, in the active matrix circuit, the channel length is 10 μm and the width of the LDD region is 0.4 to 1 μm, for instance, 0.6 μm. In an N-channel type TFT of a driver, the channel length is 8 μm, the channel width is 200 μm, and the width of the LDD region is 0.2 to 0.3 μm, for instance, 0.25 μm. In a P-channel type TFT of the driver, the channel length is 5 μm, the channel width is 500 μm, and the width of the LDD region is 0 to 0.2 μm, for instance, 0.1 μm. In an N-channel type TFT of a decoder, the channel length is 8 μm, the channel width is 10 μm, the width of the LDD regions is 0.3 to 0.4 μm, for example, 0.35 μm. In an P-channel type TFT of a decoder, the channel length is 5 μm, the channel width is 10 μm, and the
width of the LDD region is 0 to 0.2 μm, for instance, 0.1 μm. Further, in NTFTs and PTFTs of the CPU, input port, correction memory, and memory shown in Fig. 6, the width of the LDD region may be optimized in the same manner as in those of the high-frequency operation, low-electric power-consumption decoder. In this manner, the electro-optical device 74 can be formed on a single substrate having an insulating surface.

[0142]

The present invention is characterized in that 2 to 4 kinds or more of widths of the high-resistivity region can be used for the respective purposes. Further, this region need not always be made of the same material nor have the same conductive type as the channel forming region. That is, to eliminate degradations due to hot carriers and a tradeoff among the reliability, frequency characteristic, and off-current, it is effective to form the high-resistivity region by adding a very small amount of N-type impurities in an NTFT, by adding a very small amount of P-type

impurities in a PTFT, or by selectively adding carbon, oxygen, nitrogen, or the like.
[0143]

It is desirable to use the TFTs described in Figs. 3 to 5 as TFTs in the driver circuit for driving TFTs that is formed in the pixel electrodes.

[0144]

Embodiment 8

This embodiment is characterized in that it is formed by a manufacturing process described schematically below.

(1) The crystallinity of a silicon film crystallized in the step (1) is accelerated by laser light irradiation.

(2) After forming a gate electrode, source and drain regions are formed by introducing impurity ions with the gate electrode used as a mask.

(3) A heat treatment is performed to re-crystallize the source and drain regions and activate the introduced impurities.

As described above, this embodiment is characterized by the laser light irradiation and the heat treatment. The laser light irradiation is to accelerate crystallization of an amorphous silicon film, and the subsequent heat treatment is to re-crystallize the source and drain regions, activate impurities introduced into those regions, and eliminate defects in the channel forming region.

[0145]

A description will be made of a TFT manufacturing process shown in Figs. 9. First, a 2,000 Å thick undercoat silicon oxide film 902 is formed on a glass substrate 901 by sputtering, and a 1,000 Å thick amorphous silicon film is formed thereon by plasma CVD method or reduced-pressure thermal CVD method. Nickel element is then introduced into the surface of the amorphous silicon film by using nickel acetate.
[0146]

Thereafter, in a state that the sample is heated to 500°C, the crystallinity of a crystalline silicon film 903 is accelerated by irradiating it with XeCl excimer laser (wavelength: 308 nm), XeF excimer laser at an irradiation intensity 300 mJ/cm^2. (Fig. 9(A))

[0147]

Then, the crystalline silicon film 903 is patterned to form an active layer of the TFT. After a 1,000 Å thick silicon oxide film to become a gate insulating film is formed by plasma CVD method, a 5,000 Å thick film mainly made of aluminum is formed and then patterned into a gate electrode 905. Oxide layer 906 is formed around the gate electrode 905 by performing anodic oxidation in an electrolyte with the gate electrode 905 used as the anode. In this embodiment, the thickness of this oxide layer 905 is 2000 Å.

[0148]

Thereafter, a source region 907, a drain region 911, a channel forming region 909, and offset gate regions 908 and 910 are formed in a self-aligned manner by introducing impurity ions with the gate electrode 905 and the oxide layer 906 around

it used as a mask. To obtain an N-channel type TFT, phosphorus ions are used as impurity ions. In this step, the source region and the drain region are rendered amorphous by the impact of ions. (Fig. 9(B))

[0149]

In step (C), the source region 907 and the drain region 911 are re-crystallized and the introduced phosphorus ions are activated by performing a heat treatment at 500°C for 2 hours. In this step, crystal growth indicated by arrows 912 proceeds from the boundary between the crystalline offset gate region 908 and the amorphous source region 907. This crystal growth proceeds with the gate offset regions 908 serving as nuclei. Samely, the crystal growth indicated by arrows 912 proceeds from boundary between the offset gate region 910 and the amorphous drain region 911. This crystal growth proceeds easily at 500°C or less by virtue of action of phosphorus ions that have been introduced into the source region and the drain region. Since continuous crystal structures can be obtained from the offset gate regions, defect concentration due to lattice mismatching can be prevented.

[0150]

The heat treatment step conducted in the step (C) may be performed at 300°C or more. In this embodiment, since the gate electrode is made of aluminum and the heat resistance problem should be considered, the heat treatment may be performed at a temperature of 300 to 600°C.

[0151]

Also, in the heat treatment step shown in (C), it is effective to perform annealing by irradiation with laser light or intense light before or after the heat treatment step.

[0152]

Subsequently, a 6,000 Å thick interlayer insulating film is formed by plasma CVD, and a source electrode 914 and a drain electrode 915 are formed. Hydrogenation is then performed by a heat treatment in a hydrogen atmosphere of 350°C, thereby the TFT shown in (D) is completed.

[0153]

This embodiment is directed to the case of forming the offset gate regions 908 and 910. Where no offset gate regions are formed, crystallization proceeds from the channel forming region having crystallinity to the source and drain regions in the heat treatment step of (C).

[0154]

[Embodiment 9]

This embodiment relates to a configuration of an active matrix type liquid crystal display device. As shown in Fig. 10, an active matrix type liquid crystal display device of this embodiment has a pixel region arranged in a matrix shape and a peripheral circuit region for driving the pixel region.

[0155]

TFTs as switching elements are provided for the respective pixels in the pixel

region arranged in a matrix form. Also, the peripheral circuits are also constituted of TFTs.

[0156]

This embodiment is characterized in that the TFTs constituting the pixel region are formed by not using a metal element and the TFTs constituting the peripheral circuits are formed by using a metal element.

[0157]

In general, TFTs constituting a pixel region are not required to have a high mobility, but are required to have sufficient stability of characteristics and low off-current characteristics. On the other hand, TFTs constituting peripheral circuits region are required to allow a large current to flow and have a high mobility.

[0158]

In the configuration shown in the present embodiment, the TFTs constituting the peripheral circuits is formed by using a crystalline silicon film using nickel, which can provide a high mobility. On the other hand, the TFTs formed on the portion of the pixel region is made of a crystalline silicon film that has been formed by laser annealing and therefore cannot provide a high mobility but can provide a low off-current.

[0159]

To realize the above configuration, nickel element may be selectively introduced into only in silicon films that constitute the peripheral circuit region. Alternatively, the manufacturing step shown in Fig. 4 may be employed in manufacturing thin film transistors that constitute the peripheral circuit region.

[0160]

[EFFECT]

A crystalline silicon film can be obtained by introducing a catalyst element and then performing irradiation with laser light or intense light. Further, heat treatment is performed, thereby the number of defects in the silicon film can be reduced. Then, by using thus obtained crystalline silicon film to manufacture a semiconductor device, the device having superior characteristics can be obtained with good productivity.

In particular, by using an interstitial catalyst element as typified by Ni, the following advantages can be obtained:

(1) A crystalline silicon film having uniform crystallinity, i.e., not having crystal grain boundaries in particular regions. Then, by using this crystalline silicon film, a large number of TFTs having uniform characteristics which can be used in, for instance, an active matrix type liquid crystal display device can be formed on a single plane.

(2) A crystalline silicon film produced by controlling the crystal growth direction can be obtained, so that a TFT having necessary characteristics can be formed.

[BRIEF DESCRIPTION OF THE DRAWINGS]

Figs. 1 show steps of embodiment.

Figs. 2 show steps of embodiment.
Figs. 3 show manufacturing steps of embodiment.
Figs. 4 show manufacturing steps of embodiment.
Figs. 5 show manufacturing steps of embodiment.
Figs. 6 show manufacturing steps of embodiment.
Fig. 7 shows a configuration of embodiment.
Fig. 8 shows results of ESR measurements.
Figs. 9 show manufacturing steps of embodiment.
Fig. 10 shows a configuration of an active matrix type liquid crystal display device of embodiment.

[DESCRIPTION OF MARKS]

11 . . . . glass substrate
12 . . . . amorphous silicon film
13 . . . . silicon oxide film
14 . . . . acetate solution film containing nickel
15 . . . . spinner
21 . . . . silicon oxide film for mask
20 . . . . silicon oxide film
11 . . . . glass substrate
104 . . . . active layer
105 . . . . silicon oxide film
106 . . . . gate electrode
109 . . . . oxide layer
108 . . . . source/drain region
109 . . . . drain/source region
110 . . . . interlayer insulating film (silicon oxide film)
112 . . . . electrode
113 . . . . electrode

[NAME OF DOCUMENT]

[ABSTRACT]

[PURPOSE] In a method of forming a crystalline silicon film by heat treatment at around 550°C for about 4 hours by using a catalyst element for accelerating crystallization, a heat treatment is performed with a laser irradiation.

[STRUCTURE]

A very thin oxide film 13 is formed on an amorphous silicon film 12 formed on a glass substrate 11, and an aqueous solution 14 such as an acetate solution added with a catalyst element such as nickel by 10 to 200 ppm (adjustment needed) is dropped thereon. After the structure is held in this state for a predetermined period, spin drying is performed by using a spinner. A crystalline silicon film is obtained by subjecting the structure to a heat treatment of 550°C and 4 hours and then to laser light irradiation. A crystalline silicon film having a smaller defect density is obtained by further performing a heat treatment of 550°C and 4 hours.

[SELECTED DRAWING] Fig. 1